

FIG. 1

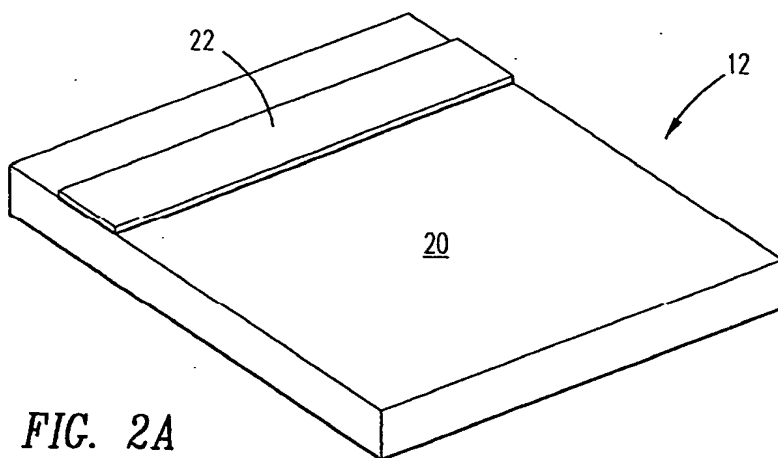


FIG. 2A

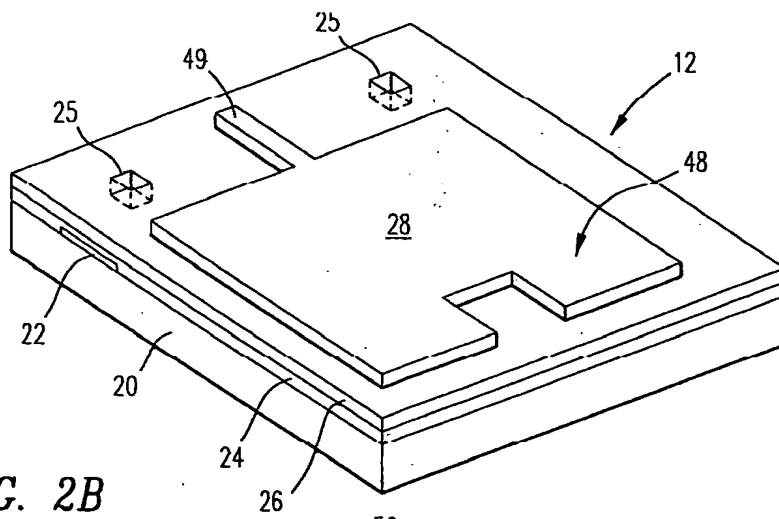


FIG. 2B

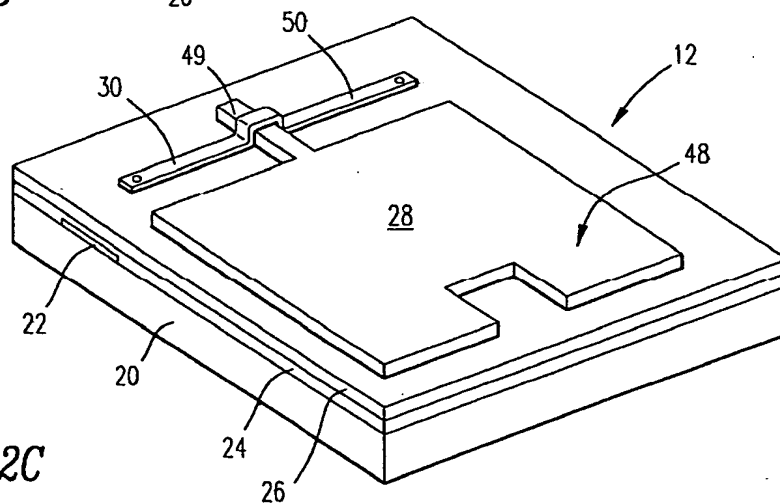


FIG. 2C

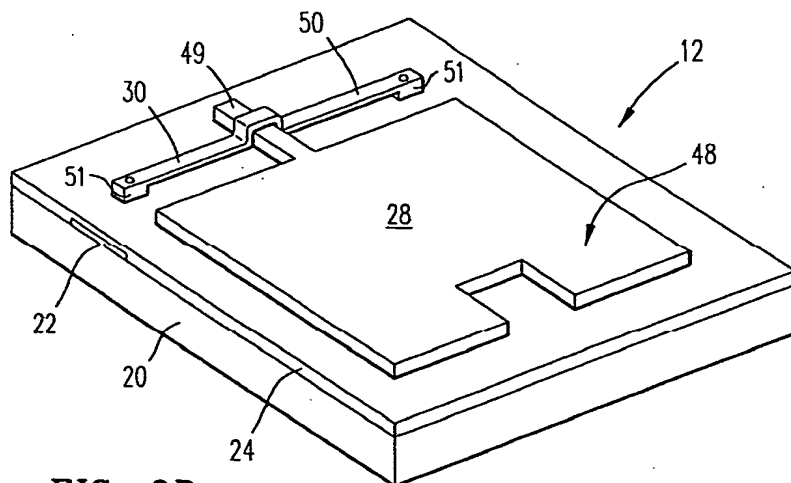


FIG. 2D

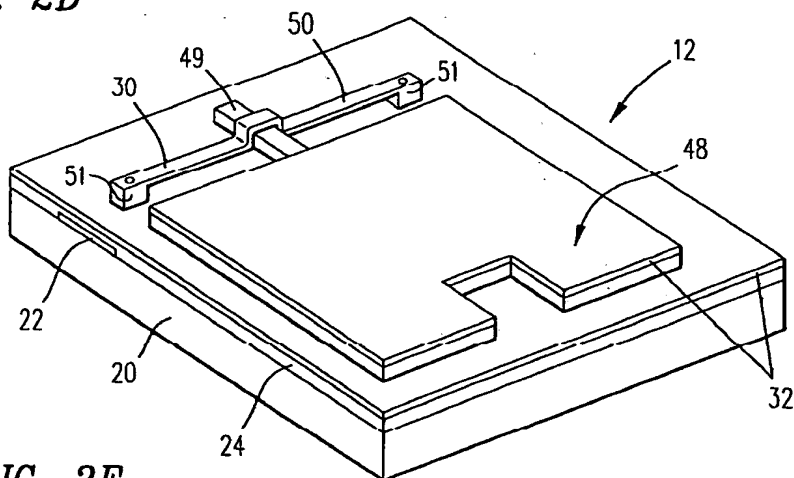


FIG. 2E

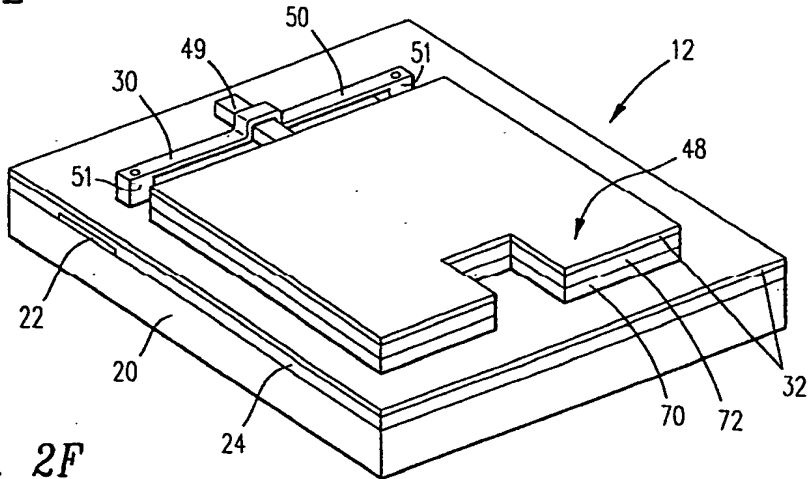


FIG. 2F

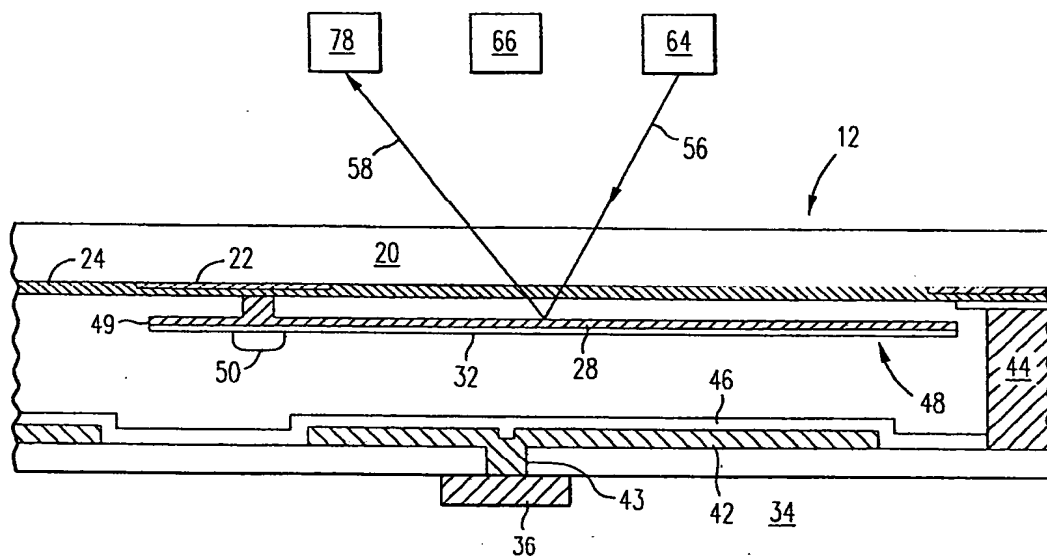


FIG. 3A

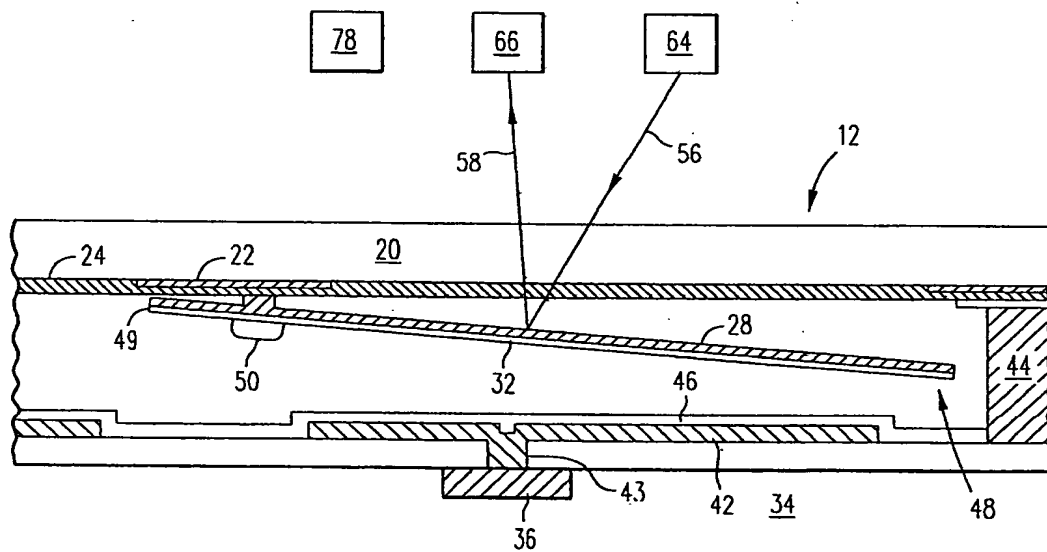
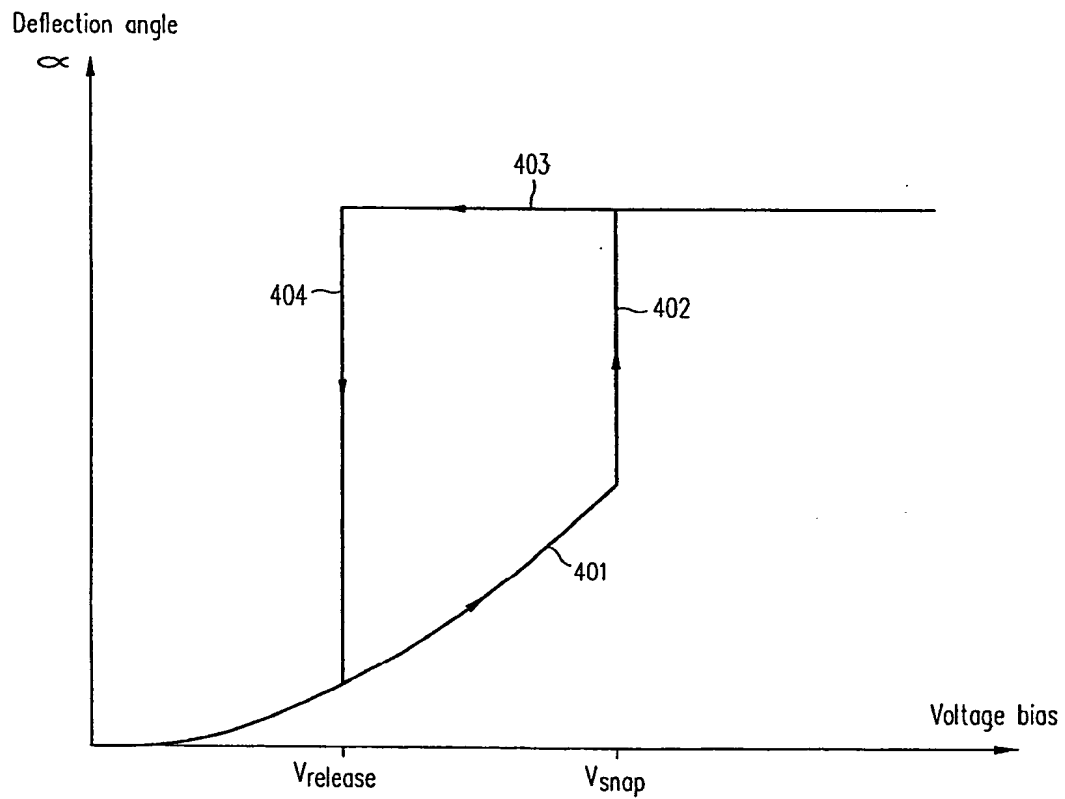


FIG. 3B



*FIG. 4*

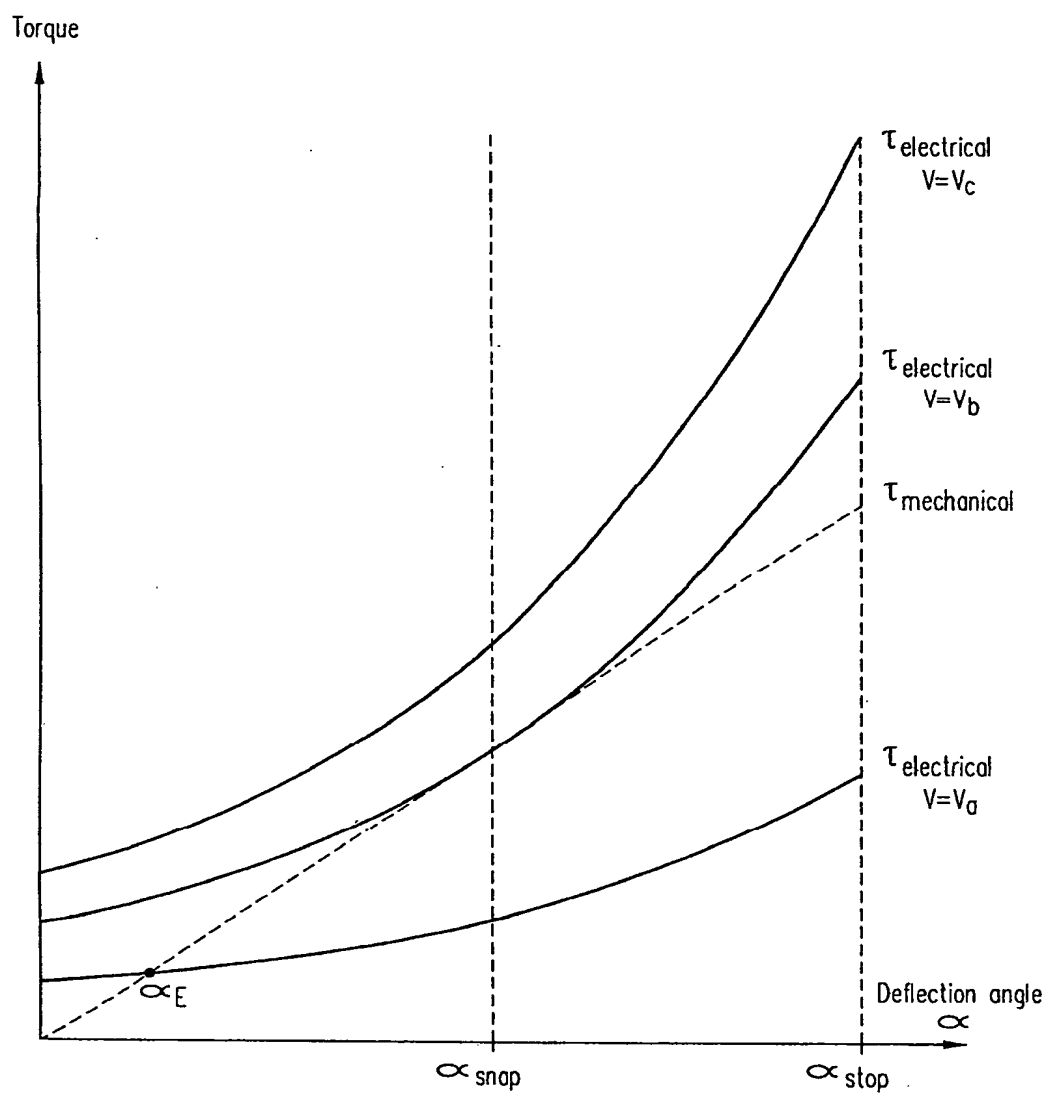


FIG. 5

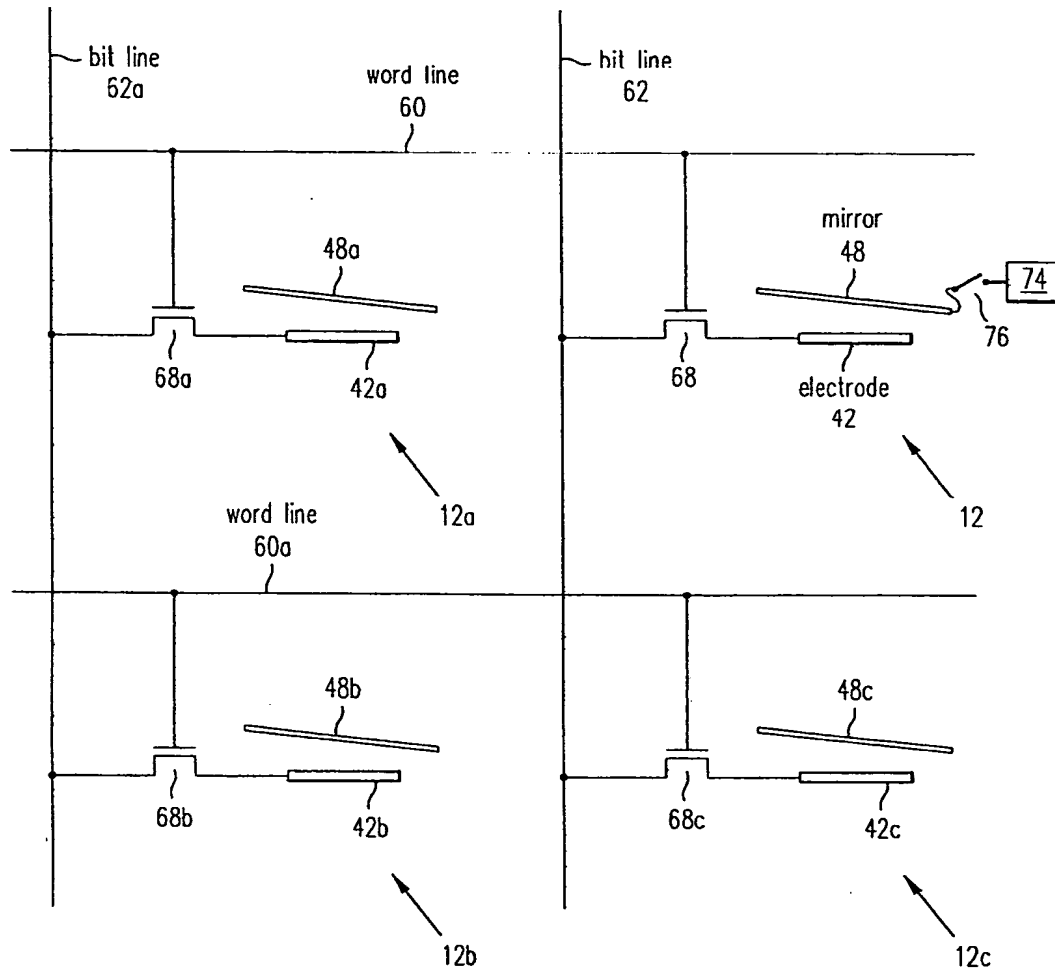
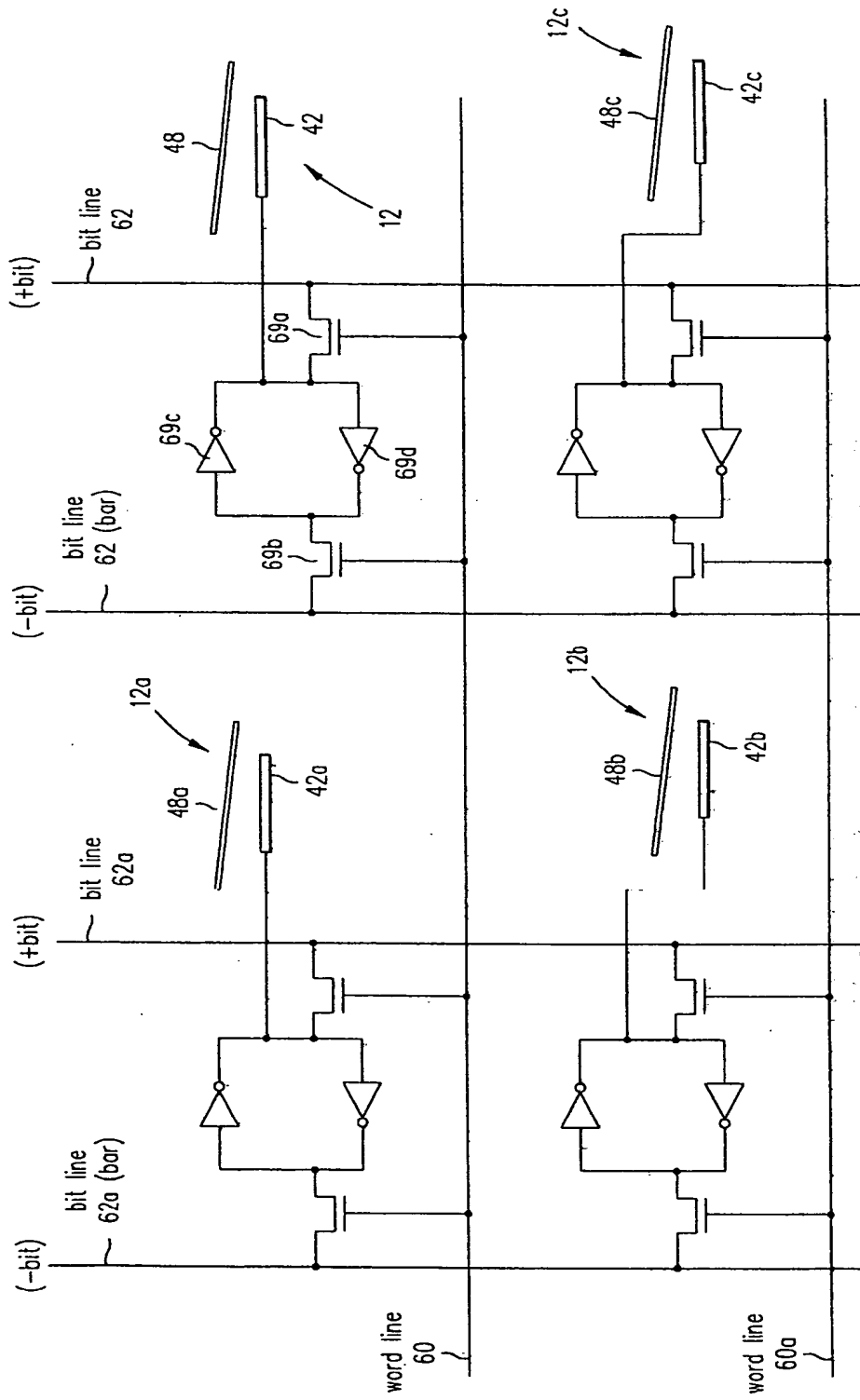


FIG. 6A



SRAM Implementation

FIG. 6B



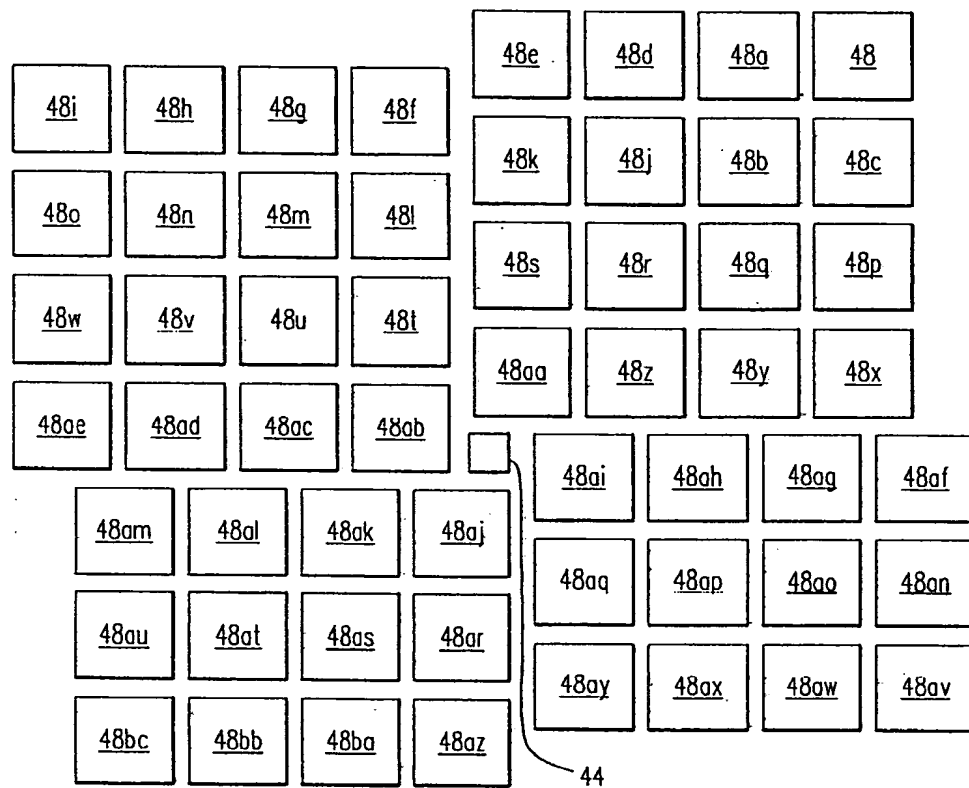


FIG. 7

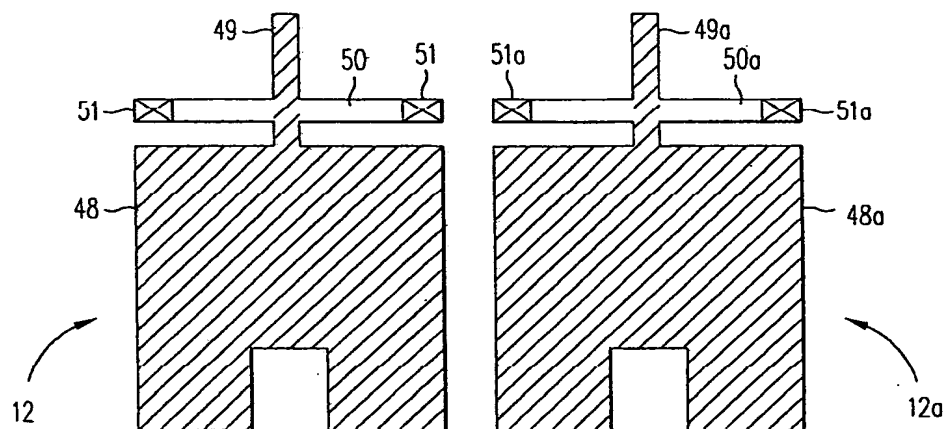


FIG. 8A

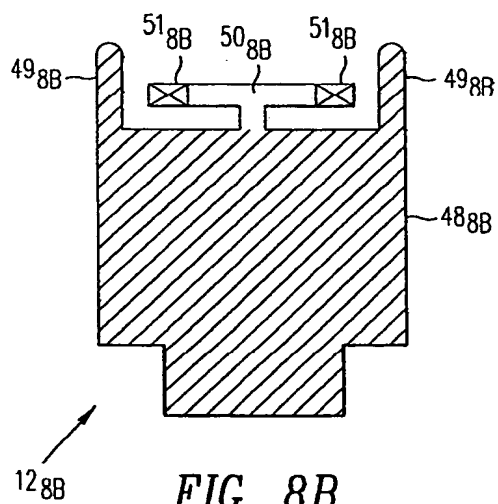
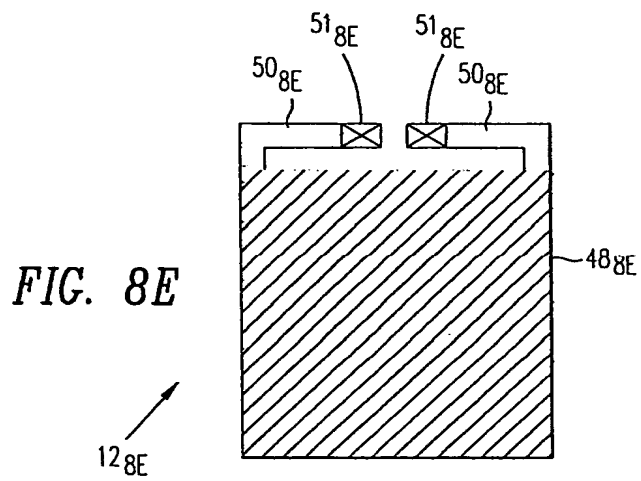
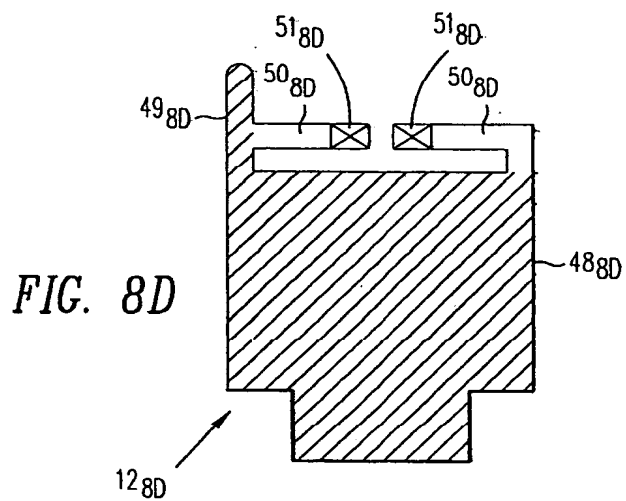
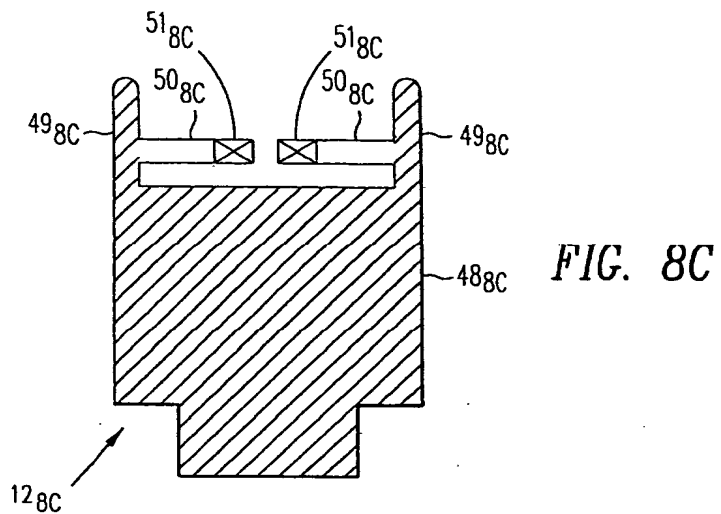
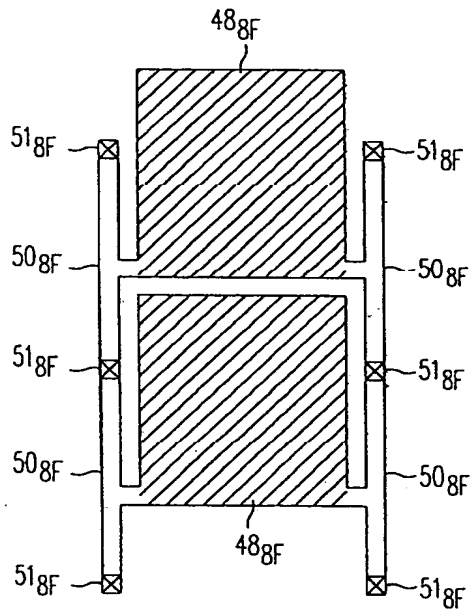
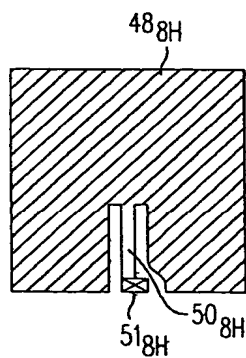


FIG. 8B

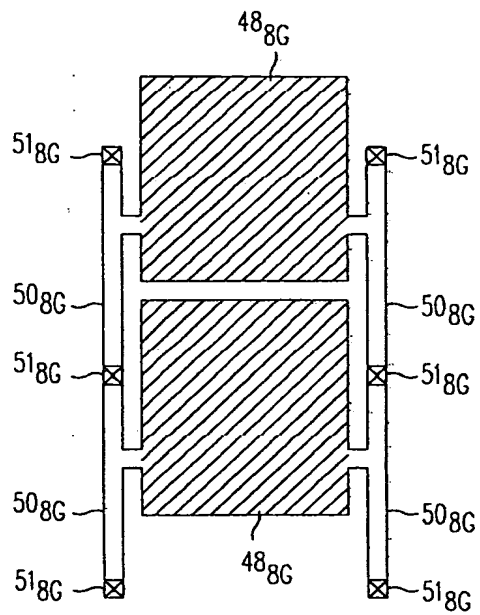




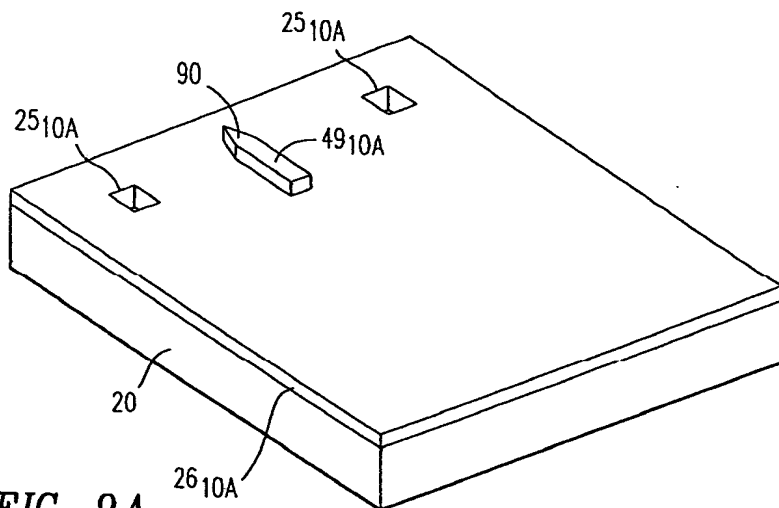
*FIG. 8F*



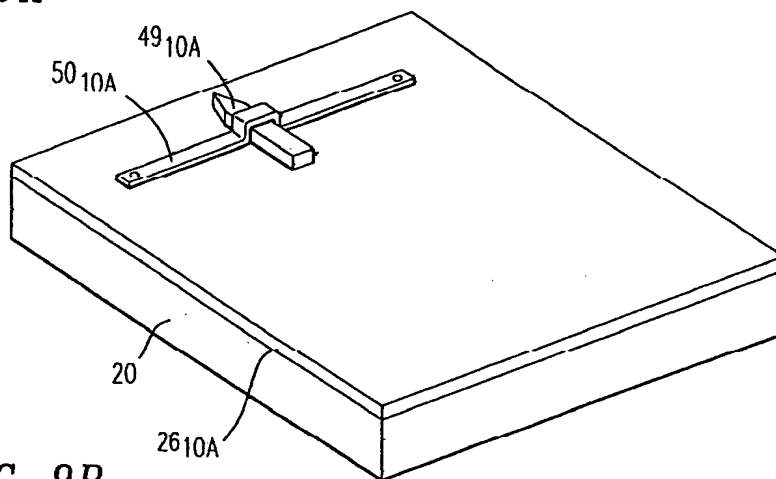
*FIG. 8H*



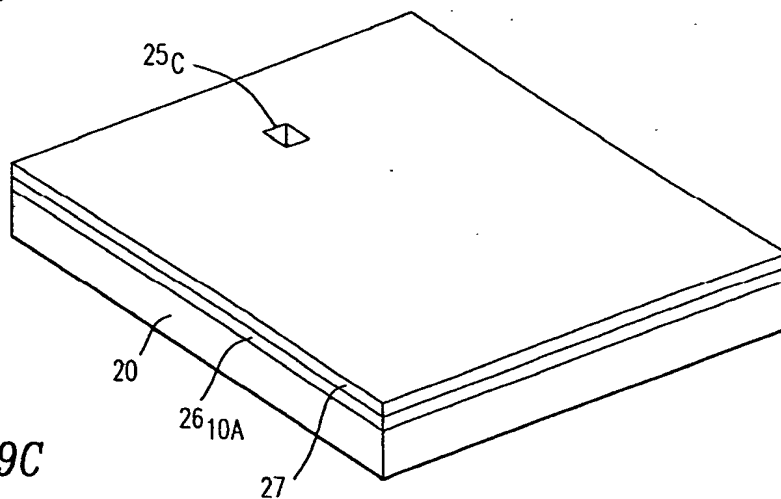
*FIG. 8G*



**FIG. 9A**



**FIG. 9B**



**FIG. 9C**

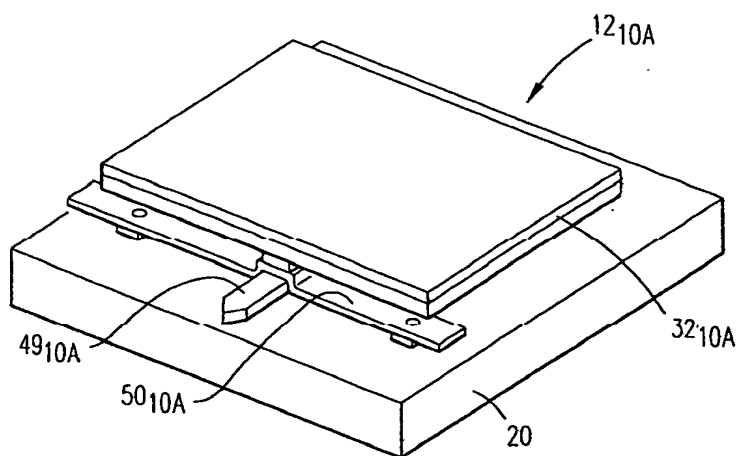


FIG. 10A

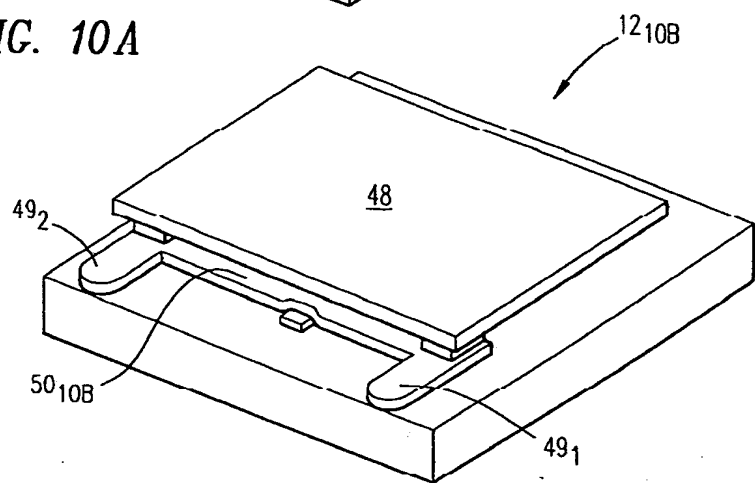


FIG. 10B

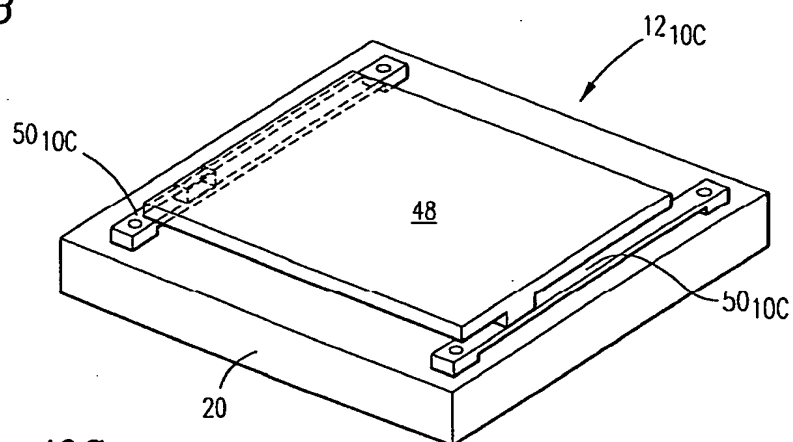
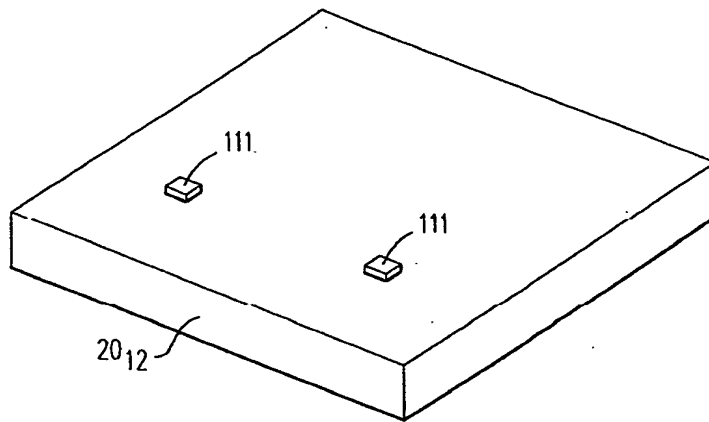
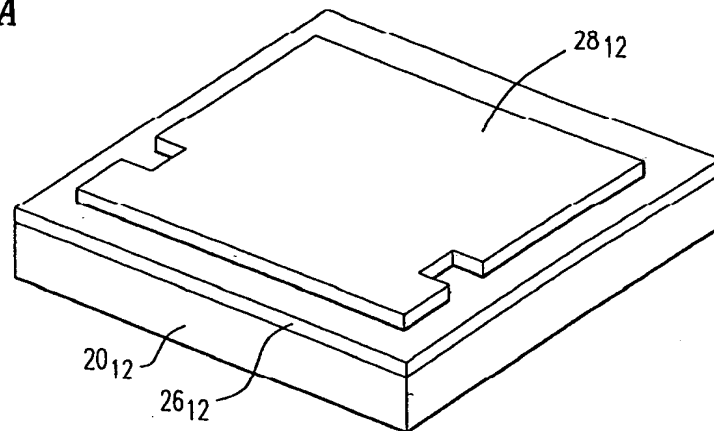


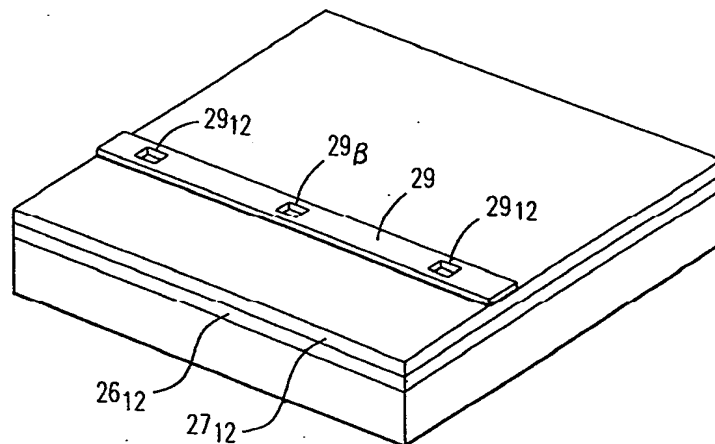
FIG. 10C



**FIG. 11A**



**FIG. 11B**



**FIG. 11C**

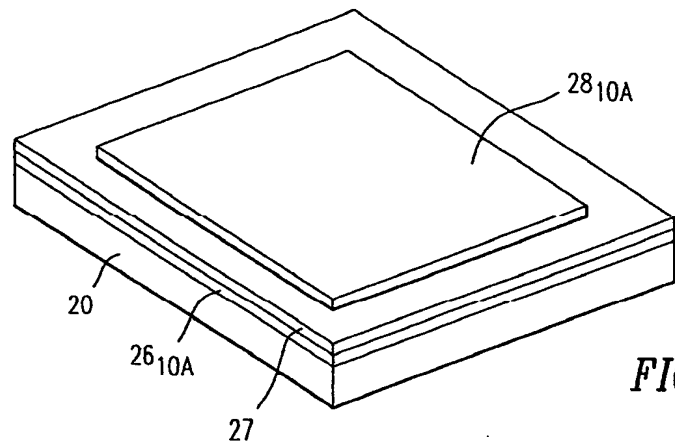


FIG. 9D

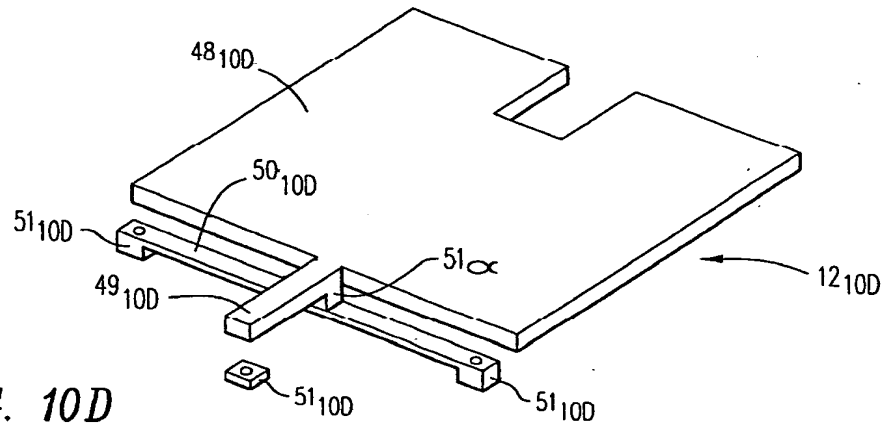


FIG. 10D

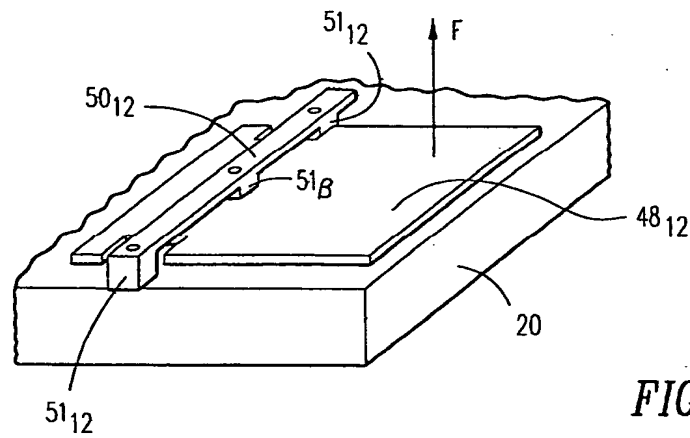


FIG. 12



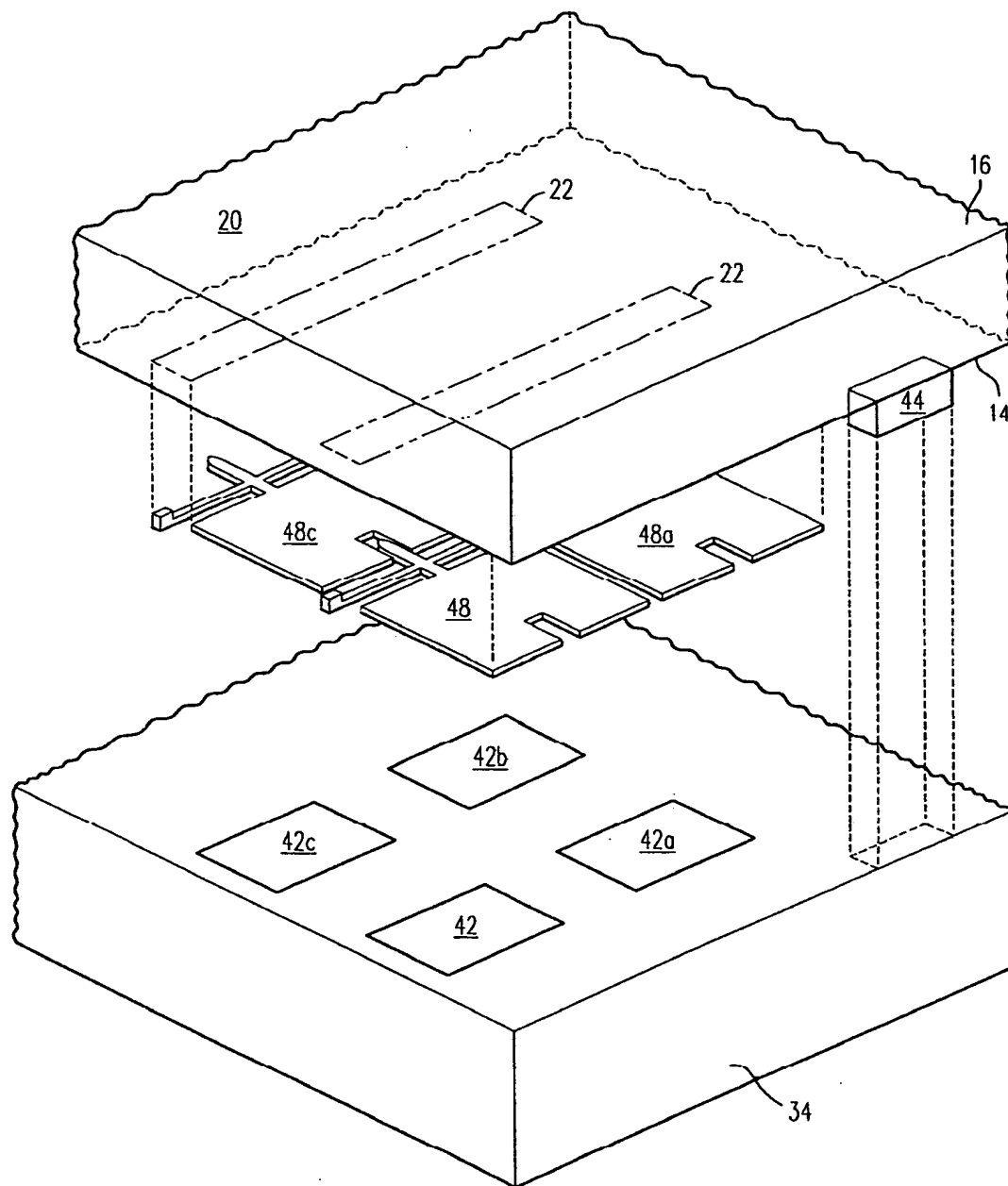


FIG. 13

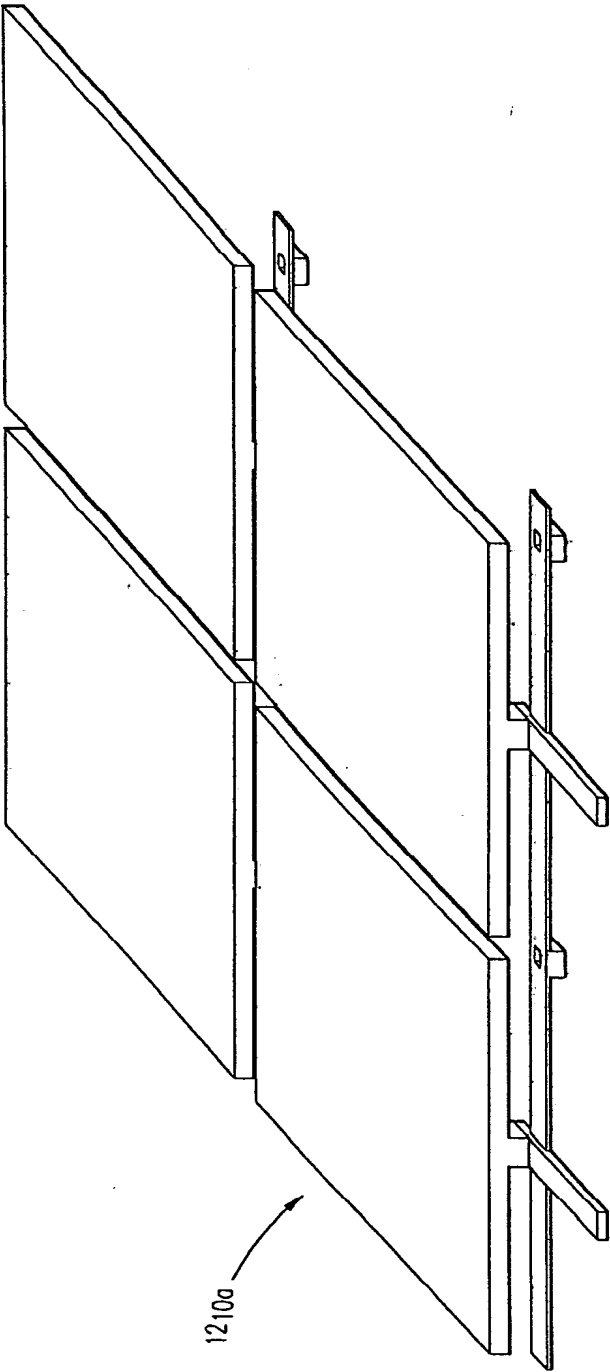


FIG. 14